IN THE SPECIFICATION:

Please replace Paragraph **[0003]** as follows:

[0003] State of the Art: Dynamic random access memory, otherwise known as a DRAM memory chip, die, or device, is a popular type of semiconductor memory device. A DRAM memory device is essentially multiple arrays formed by a series of memory cells including a transistor, such as a metal oxide semiconductor field effect transistor (MOSFET) and an associated capacitor connected thereto fabricated on a substrate, such as a silicon substrate. The memory cells are combined with peripheral circuits to form the DRAM device. The state of the memory cell, either charged or uncharged, represents the state of a binary storage element, zero or one, (data) stored by the DRAM device in the memory cell. Multiple capacitors on a single silicon substrate or chip are therefore capable of storing large amounts of data. The greater the number of capacitors formed on a substrate or chip, the greater the memory capabilities of the DRAM memory device.

Please replace Paragraph **[0009]** as follows:

[0009] Alternating layers of Ge-BPSG and BPSG, or NSG, are deposited on electrical contacts of a DRAM memory device or [Metal Oxide Semiconductor Field Effect Transistor]metal oxide semiconductor field effect transistor (MOSFET) using chemical vapor deposition (CVD) processes or plasma enhanced chemical vapor deposition processes (PECVD) using suitable apparatus operating at either atmospheric pressure levels or sub-atmospheric pressure levels. The layers are deposited in clusters such that individual capacitance cells are formed having trenches or spaces between each capacitance cell. Once the desired capacitance cell thickness is reached, the capacitance cells are capped with an etch-resistant layer. Introduction of either a wet or dry etchant into the trenches between the capacitance cells, however, etches the alternating layers at varying rates, thereby forming the rippled or corrugated wall of each capacitor cell. The form of the rippled or corrugated configuration of the capacitor cell wall is dependent upon the etch rates of the alternating layers, and specifically on the concentration of germanium (Ge) in the Ge-BPSG layers forming the capacitor cell.